A CMOS Dual-band Tri-mode Chipset for IEEE 802.11a/b/g Wireless LAN

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Abstract — **This paper presents the design of a dual-band, tri-mode wireless LAN chipset for IEEE 802.11a/b/g. The chipset, designed in 0.25µm standard CMOS, features a 5GHz RF transceiver, a 2.4GHz RF transceiver, and a baseband processor with media access controller. The overall design achieves a measured sensitivity of at least –70dBm at 54Mbps and –92dBm at 6Mbps for IEEE 802.11a/g as well as –94dBm at 1Mbps for 802.11b.**

I. Introduction

The growth of the wireless LAN (WLAN) market for offices and homes has led to the proliferation of a multitude of WLAN standards. The evolving WLAN landscape has created the need for a flexible radio architecture that can support the existing installed base as well as embrace new standards as they emerge. The major challenge of such a flexible radio is the ability to operate at a wide radio frequency (RF) range and a varied dynamic range while preserving power efficiency and maintaining low cost. CMOS process technology has proven to be a viable candidate for a low-cost radio solution due to its compatibility with high levels of integration.

II. Architecture

The architecture chosen for this multi-standard WLAN chipset maximizes the sharing and reuse of circuit blocks to reduce overall die area. Fig. 1 shows a block diagram of the solution. It consists of three chips: a baseband processor, a 5GHz transceiver, and a 2.4GHz transceiver, all of which are implemented in a 0.25µm standard CMOS process with 2.5V core supply voltage and 3.3V I/O supply voltage.

The baseband processor includes all digital physical layer (PHY) and Media Access Control (MAC) functions, as well as two 9b I/Q ADCs, two 9b I/Q DACs, and an on-chip phase locked loop (PLL) with on-chip loop filter [1]. The baseband processor also supplies all of the control signals to the two RF transceivers. The baseband PHY performs the baseband encoding and decoding for both

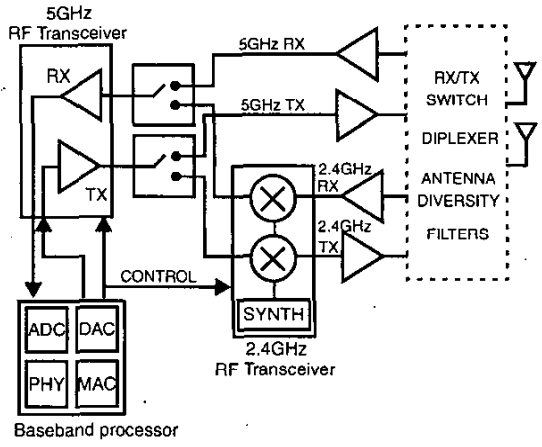

Fig. 1. Block diagram of the dual-band tri-mode IEEE 802.11a/b/g solution.

Orthogonal Frequency Division Multiplexing (OFDM) and Complementary Code Keying (CCK) modulations.

The 5GHz RF transceiver serves two functions. It is designed to translate signals between the baseband processor and 5GHz RF antenna. In addition, it is used in the 802.11b/g mode to translate signals between the baseband processor and the 2.4GHz transceiver. As shown in Fig. 1, the receiver input of the 5GHz RF transceiver comes from an off-chip LNA for 5GHz operation or from the 2.4GHz RF transceiver for 2.4GHz operation. The off-chip LNA is included to enhance performance and mitigate the degradation in noise figure (NF) due to the insertion losses from RF switches and filters. The transmitter of the 5GHz transceiver either drives an off-chip power amplifier (PA) or the 2.4GHz RF transceiver.

The function of the 2.4GHz RF transceiver in Fig. 1 is somewhat unconventional. It translates the 2.4GHz RF signals up to the 5GHz RF ports of the 5GHz transceiver,

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which then converts the signal to baseband. In this approach, the various circuit functionalities on the 5GHz transceiver, such as channel selection, filtering, offset cancellation, and automatic gain control, are not duplicated on the 2.4GHz transceiver, thereby saving die area in the overall chipset. The receiver input of the 2.4GHz RF transceiver comes from an off-chip LNA and its transmitter output drives an off-chip PA.

The 5GHz and 2.4GHz RF signals are fed to on-board switches and filters that perform transmit/receive selection, 2.4GHz/5GHz diplexing and antenna diversity.

A. 5GHz Transceiver

Fig. 2 shows a block diagram of the 5GHz RF transceiver. The transceiver converts baseband signals to and from 5GHz and operates from 4.9GHz to 5.925 GHz. It

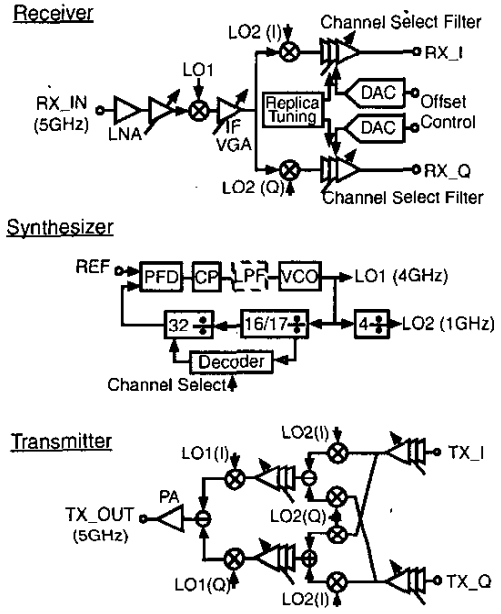

Fig. 2. Block diagram of the 5 GHz transceiver.

includes two frequency conversion steps, with adjustable gain and on-chip filtering in all frequency domains [2]. The receiver gains are adjusted digitally by the baseband processor. A continuous-time channel select filter, with on-chip tuning replica, has been incorporated to meet adjacent channel and alternate channel blocking requirements. The filter is shown in Fig. 3.

The filter transfer function is a fourth-order Butterworth lowpass, with a corner frequency which is selectable to either 11MHz (in standard mode) or 22MHz (in Atheros Turbo mode). The four filter poles are constructed by cascading two biquad (two-pole) filter sections. Each biquad is implemented using a current-mode transconductor-capacitor (gm-C) architecture, tuned by means of digitally controlled capacitor arrays. Each biquad section

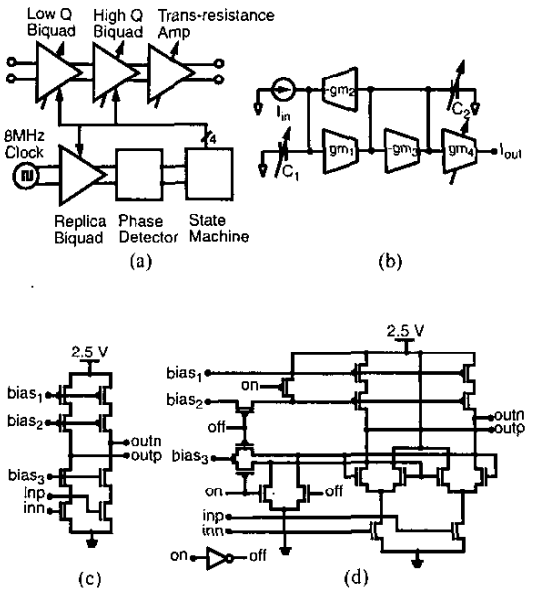

Fig. 3. Channel select filter (a) block diagram (b) gm-C biquad (c) gm cell (d) programmable gm-cell.

contains 18dB of programmable gain in 6dB steps which, when combined with a third current-to-voltage conversion stage with 5dB of programmable gain in 1dB steps, results in 41dB of total baseband programmable gain range in 1dB steps. The programmable gain in the biquad stages is implemented through digitally switched current mirrors, whereas the current-to-voltage stage consists of an op-amp trans-resistance stage with a digitally controlled resistor network. The capacitance setting required to automatically tune the cutoff frequency is selected with the combination of a replica biquad block, phase detector, and capacitor selection state machine. Cutoff frequency tuning is done by comparing the phase shift through the replica biquad to 90 degrees and adjusting the capacitance accordingly. Calibration typically takes less than 1μsec and is performed every time the receiver is turned on.

The VCO, synthesizer, and crystal oscillator are all integrated on chip. The synthesizer performs all of the channel selection for both 5GHz and 2.4GHz operation. It synthesizes channels from 4.9GHz to 5.925GHz in 5MHz incre-

ments. The VCO (LO1) runs at four-fifths of the desired frequency. The VCO is further divided by four to create I and Q LO2 signals.

A transmit power control loop supports either an internal or off-chip power detector to set the desired output power level. All of the transmit power control circuitry is implemented on-chip. In addition, each circuit block has digitally adjustable bias control so that the actual power consumption scales with system requirement. For example, in 11b or 11g mode, the 5GHz transmitter output power is scaled back to reduce power consumption when driving the 2.4GHz transceiver. The transceiver includes a LNA with 4dB noise figure (NF), and a PA that can deliver +22 dBm Psat. The overall NF without the external LNA is measured to be 5.2dB. The die area is 21.2 mm^2 and the die is packaged in a 64-pin LPCC.

B. 2.4GHz Transceiver

The 2.4GHz RF transceiver, shown in Fig. 4, provides operation in the 2.4GHz band. In receive mode, the transceiver functions as a frequency upconverter that converts the RF signals from 2.4GHz to 5.6GHz. In transmit mode, it follows the inverse operation and downconverts the 5.6GHz signal down to 2.4GHz. The RF synthesizer and

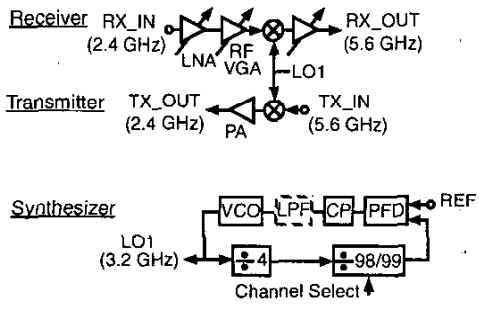

Fig. 4. Block diagram of the 2.4 GHz transceiver.

VCO are on-chip, requiring only the synthesizer passive loop filter elements off-chip. Two constraints determine the choice of 5.6GHz "intermediate frequency (IF)". First, it is desirable to separate LO1 from the desired channel to relax filtering requirements in the presence of local oscillator (LO) leak. Second, the IF should avoid the 5.25-5.35GHz U-NII middle band and the 5.725-5.825GHz U-NII upper band to minimize interference issues in systems with simultaneous 11a/b or 11a/g operation. The 5.6GHz IF falls between the middle and upper U-NII bands and allows for an LO1 at ~3.2GHz that is ~800MHz away from 2.4GHz. Table 1 shows the channel selection frequency plan. All of the channel selection is done in the 5GHz transceiver thereby allowing the 2.4GHz frequency synthesizer to have a high reference frequency and high loop bandwidth resulting in lower phase noise. For channels 1-13, the synthesizer is fixed to 3.168GHz. In channel 14, it is programmed to 3.136GHz to account for the different step.

TABLE I
SYSTEM FREQUENCY PLAN

802.11b Channel (GHz)	5GHz TX_OUT (GHz)	2.4GHz Synth (GHz)
2.412	5.580	3.168
2.417	5.585	3.168
2.422	5.590	3.168
2.427	5.595	3.168
2.432	5.600	3.168
2.437	5.605	3.168
2.442	5.610	3.168
2.447	5.615	3.168
2.452	5.620	3.168
2.457	5.625	3.168
2.462	5.630	3.168
2.467	5.635	3.168
2.472	5.640	3.168
2.484	5.620	3.136

The receiver incorporates three programmable gain stages for maximum flexibility in signal scaling. The LNA gain can be set typically to 21dB or 32dB. In maximum gain mode, the receive chain has a NF of 4.5dB. The RF variable gain amplifier (VGA) has a gain range from -12dB to 16.5dB in approximately 6dB steps, and the output buffer has 18dB of programmable attenuation in 6dB steps. The attenuation is required due to the large difference in maximum signal size, -10dBm, for 11b compared to -30dBm, for 11a.

The transceiver is designed to be used with an off-chip power amplifier. The transmitter delivers a 0dBm output signal to an off-chip PA that achieves greater than 18dBm OFDM transmit power. The die area is 12.2mm^2 and the die is packaged in a 48-pin LPCC.

III. Measurements And Results

Performance results for the overall system are shown in Table 2. The overall receiver NF, including losses due to switches and RF filtering, is 4.5dB at 2.4GHz and 5.5dB at 5GHz. The maximum saturated output power at the antenna port, including losses due to switches and RF filtering, is 23dBM at 2.4GHz and 22dBm at 5GHz. Table 2 shows a summary of the performance results. The die micrographs are shown in Fig. 5. The reference design performance in a typical office environment is shown in Fig. 6. The test setup is described in [3]. The throughput does not smoothly decrease with distance since each test location is subject to significantly different obstructions. For example, point 166 is inside a distant conference room with several concrete walls between the test location and the access point, while point 167 is in a more open area. The performance of 11a is significantly better than first generation products [2] while the performance of 11b and pre-11g is comparable to or better than current leading products. More interestingly, the range performance of 11a is substantially better than that of both 11b and 11g.

TABLE 2
SYSTEM PERFORMANCE RESULTS

Mode / Data Rate	Sensitivity (dBm)	Output Power[1] (dBm)	Total Power Consumption[2] (W)
802.11a - 6Mbps	-92	+20	1.85 (TX)[2] 1.20 (RX)
802.11a - 54Mbps	-72	+14	
802.11b - 1Mbps	-94	+21	1.75 (TX)[3] 1.29 (RX)
802.11b - 11Mbps	-89	+21	
802.11g - 6Mbps	-90	+20	1.82 (TX)[2] 1.40 (RX)
802.11g - 54Mbps	-70	+14	

[1] 10% packet error rate limited
[2] +17dBm output power
[3] +18dBm output power

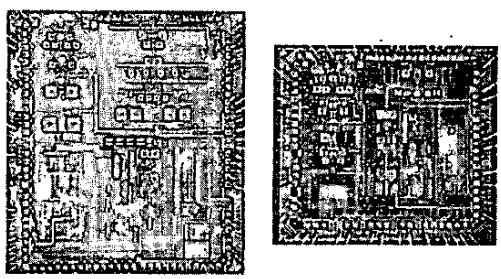

Fig. 5. Die micrographs of (a) 5GHz and (b) 2.4GHz ICs (not on same scale).

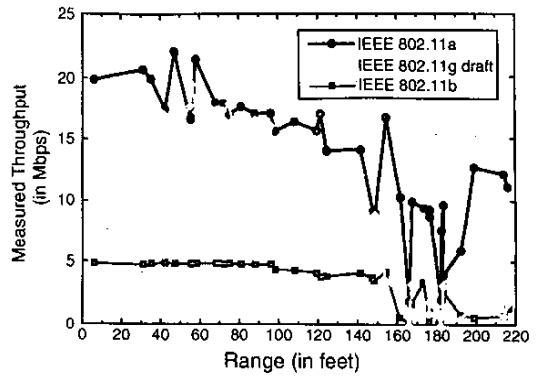

Fig. 6. Measured throughput versus range for 802.11a/b/g.

IV. Conclusion

The wireless LAN market is rapidly migrating towards multi-mode multi-band operation to achieve higher data rates and greater capacities. A chipset addressing IEEE 802.11a/b/g is presented. The unique architecture results in a low-cost, power efficient, integrated CMOS solution by maximizing the reuse of circuit blocks and conserving die area.

Acknowledgement

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